

FIG. 1A

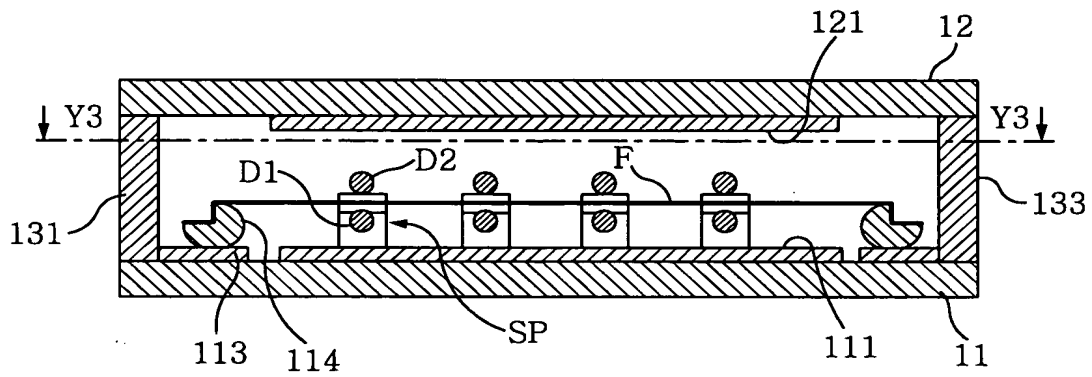


FIG. 1B

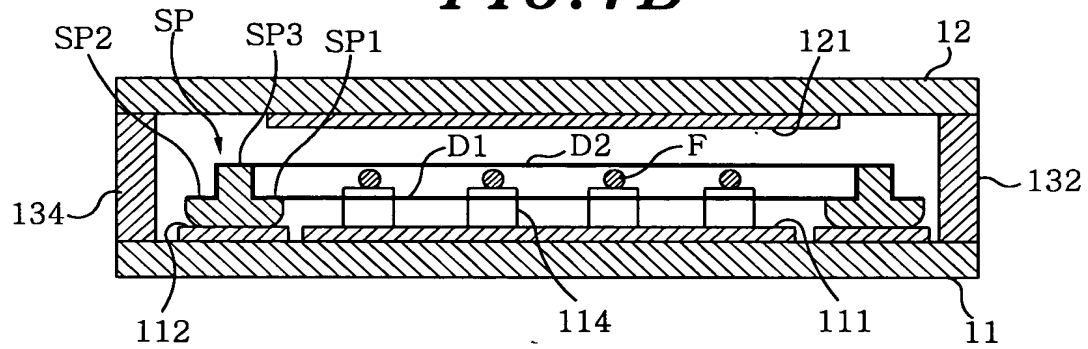


FIG. 1C

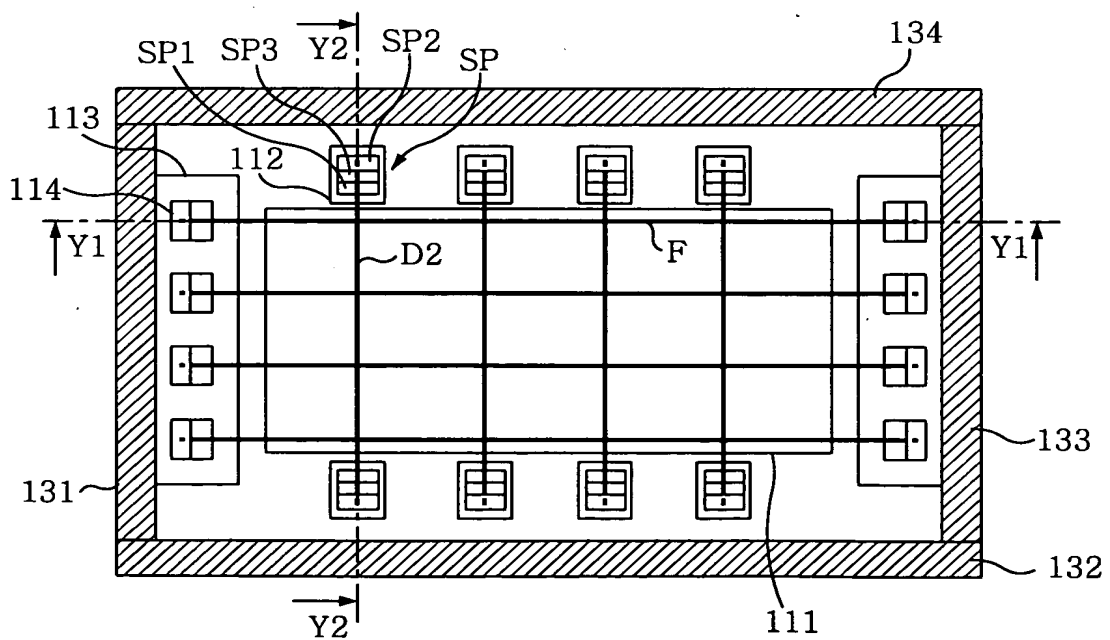


FIG. 2A

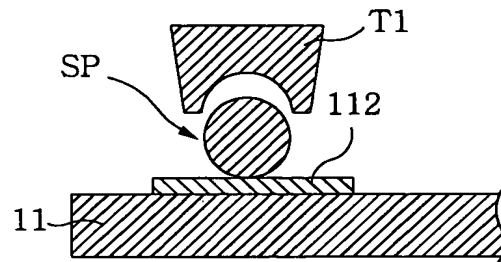


FIG. 2B

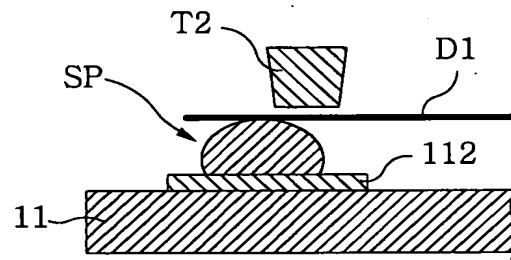


FIG. 2C

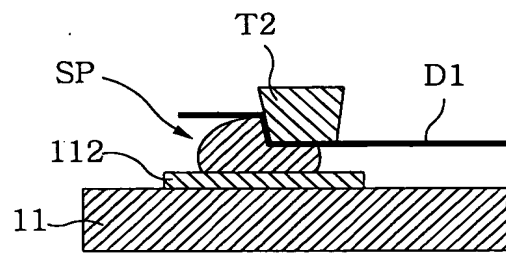


FIG. 2D

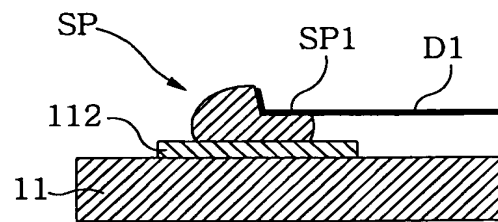


FIG.2E

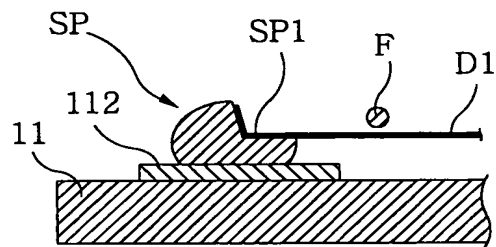


FIG.2F

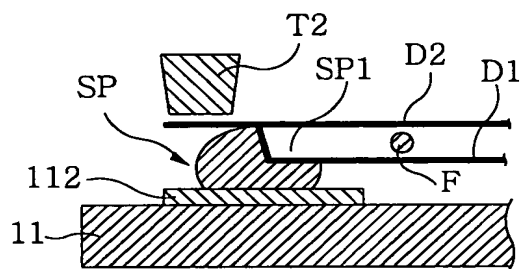


FIG.2G

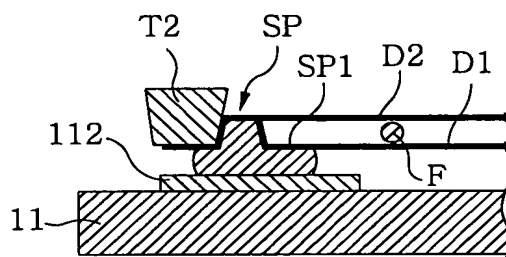


FIG.2H

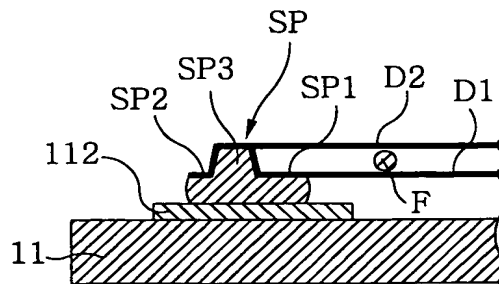


FIG. 4A

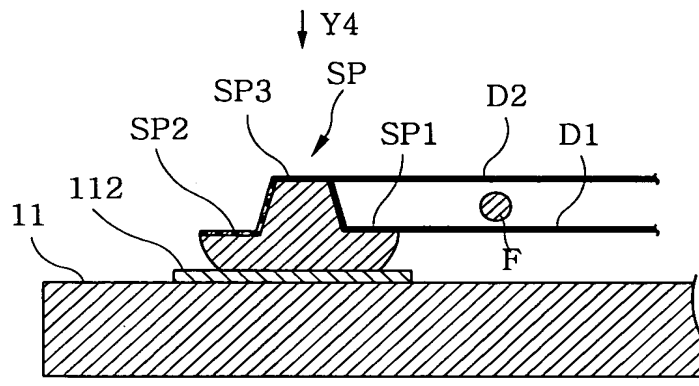


FIG. 4B

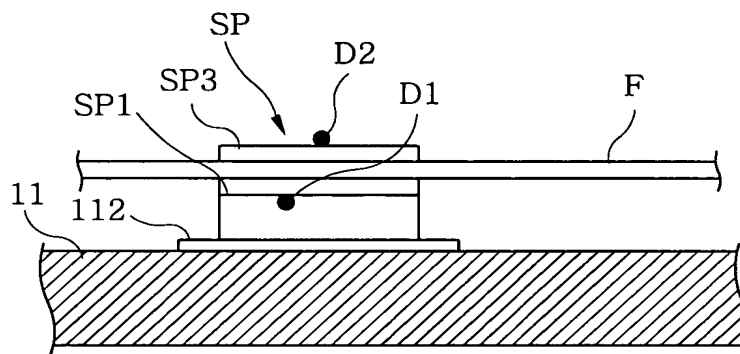


FIG. 4C

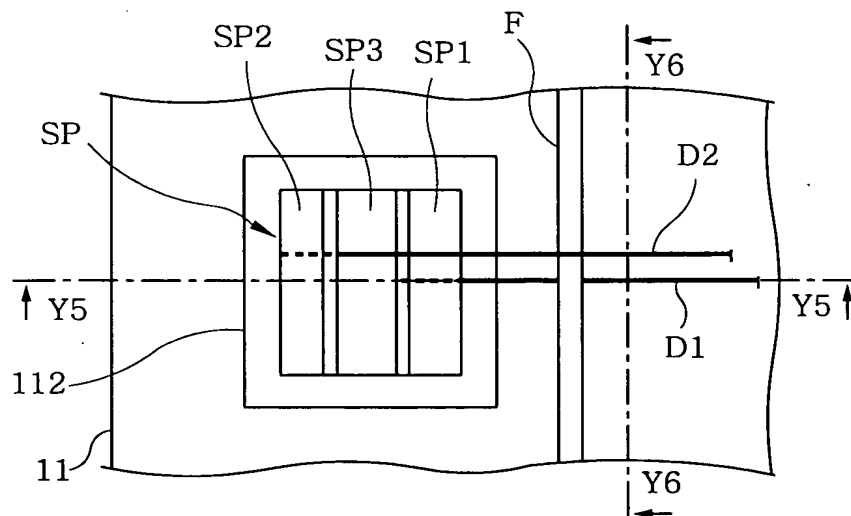


FIG. 5A

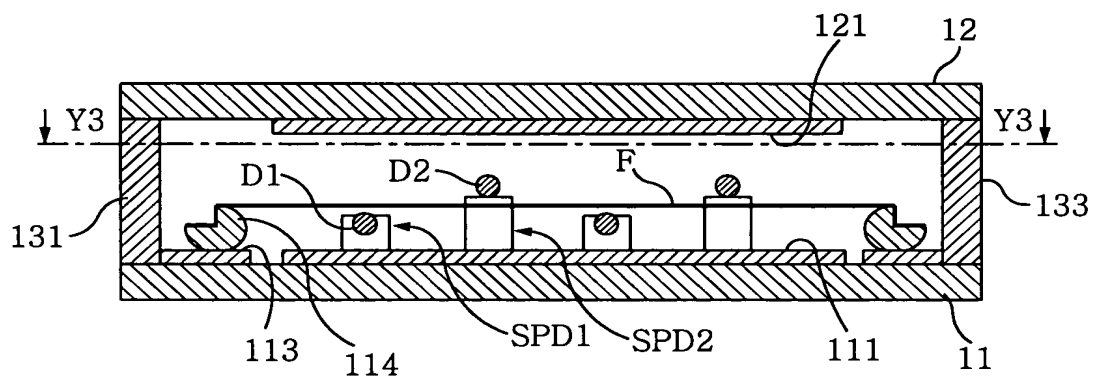


FIG. 5B

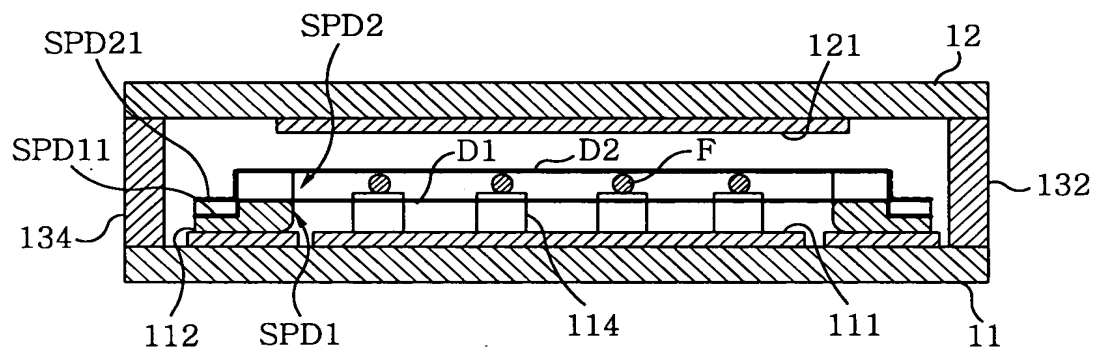


FIG. 5C

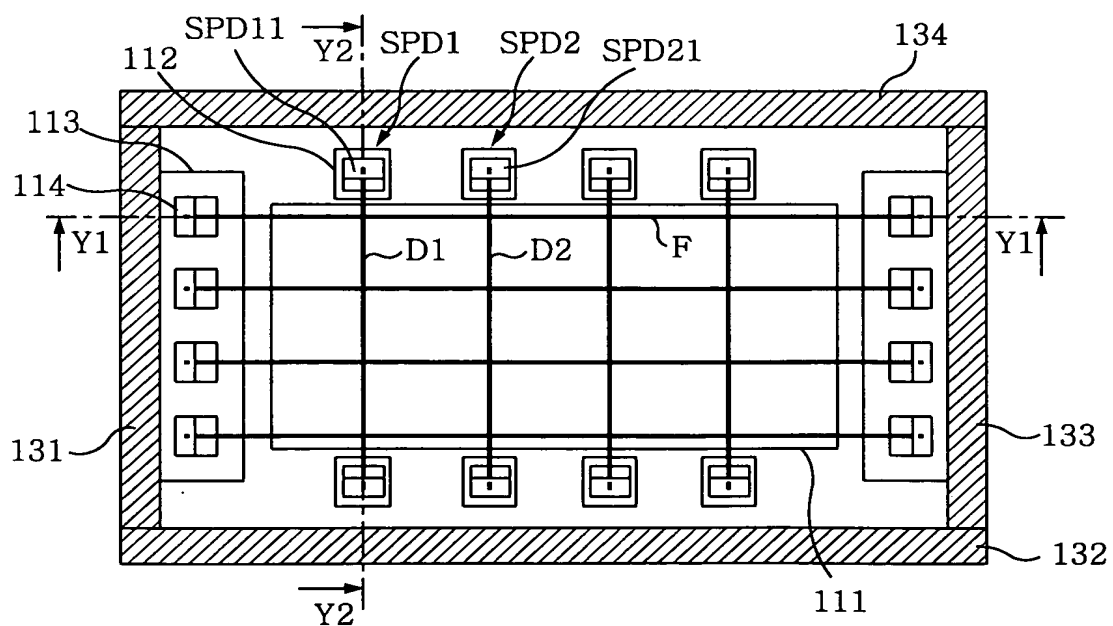


FIG. 6A

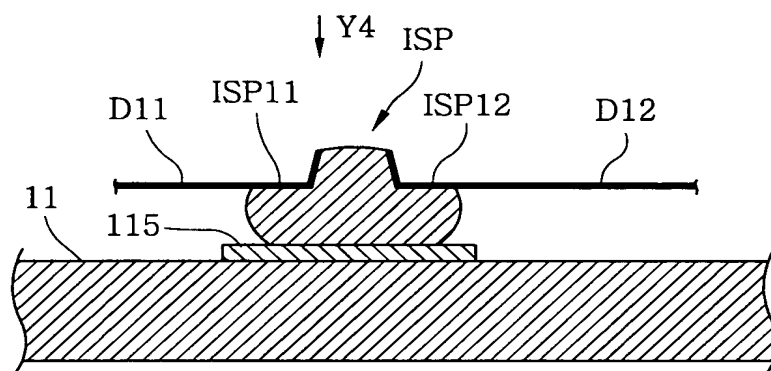


FIG. 6B

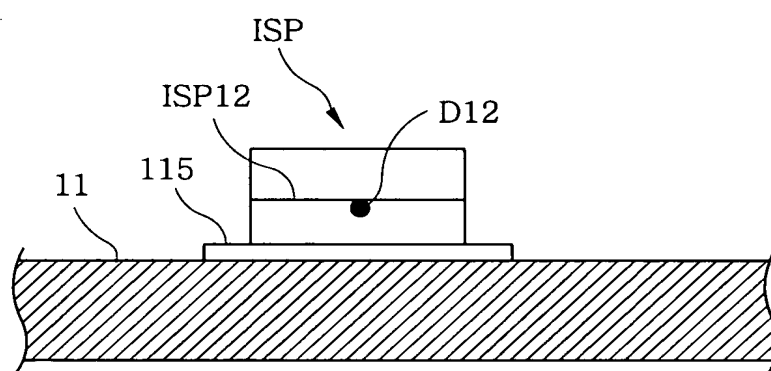


FIG. 6C

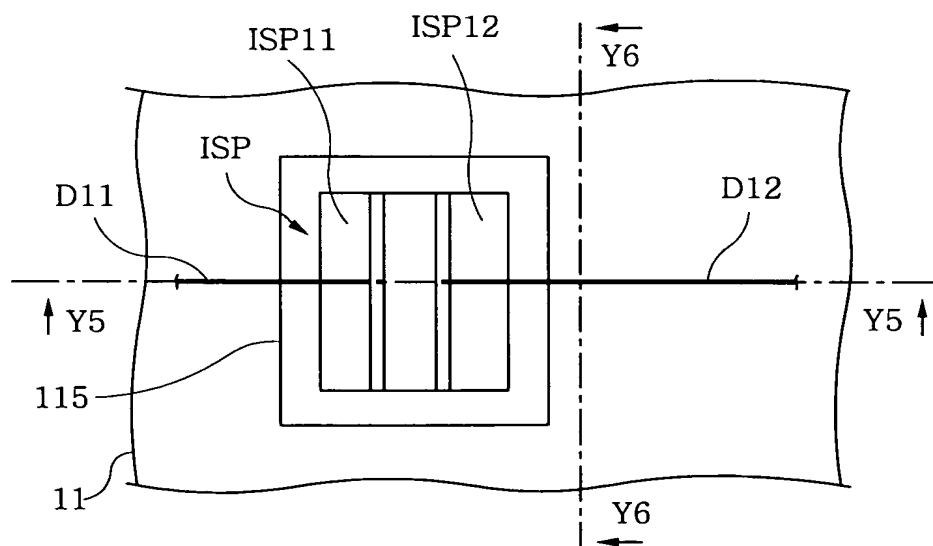


FIG. 7A

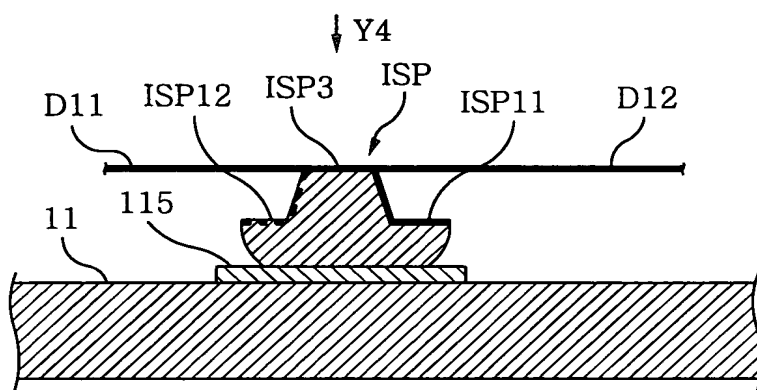


FIG. 7B

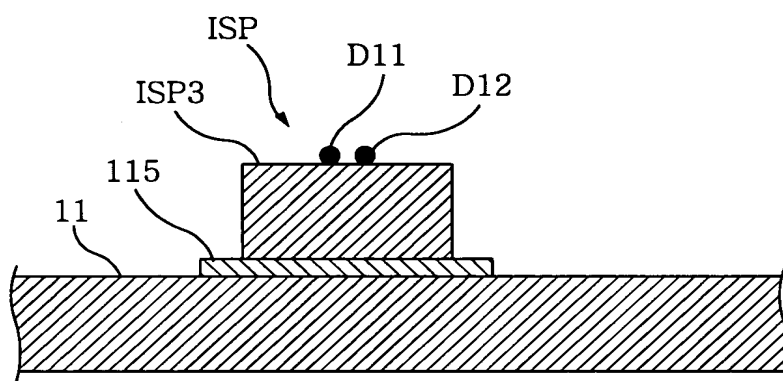
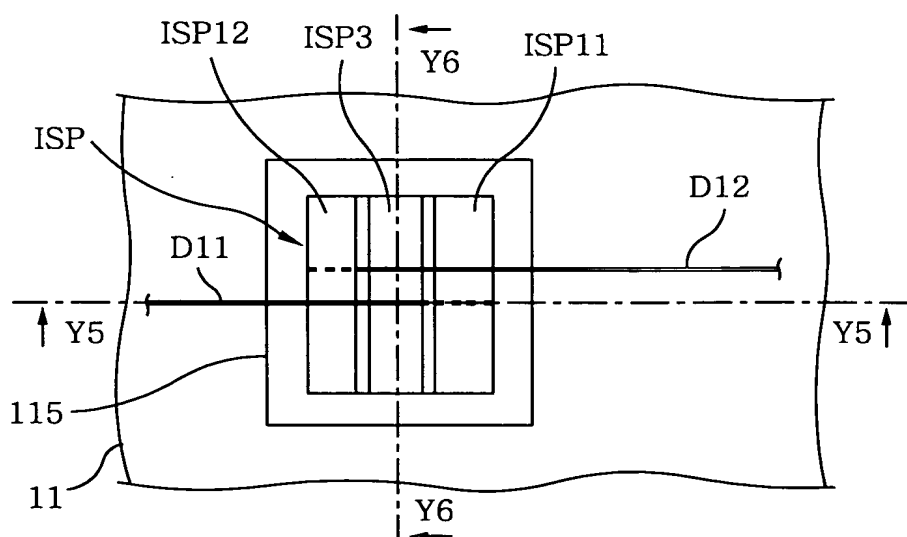


FIG. 7C



[illegible]

A cross-sectional view of a semiconductor device. A substrate 11 is shown at the bottom. A layer 112 is formed on the substrate. A contact pad 1513 is formed on the layer 112. A wire 1514 is formed on the contact pad 1513. Two vias, D1 and D2, are formed in the wire 1514. A force F is applied to the wire 1514.

FIG. 10

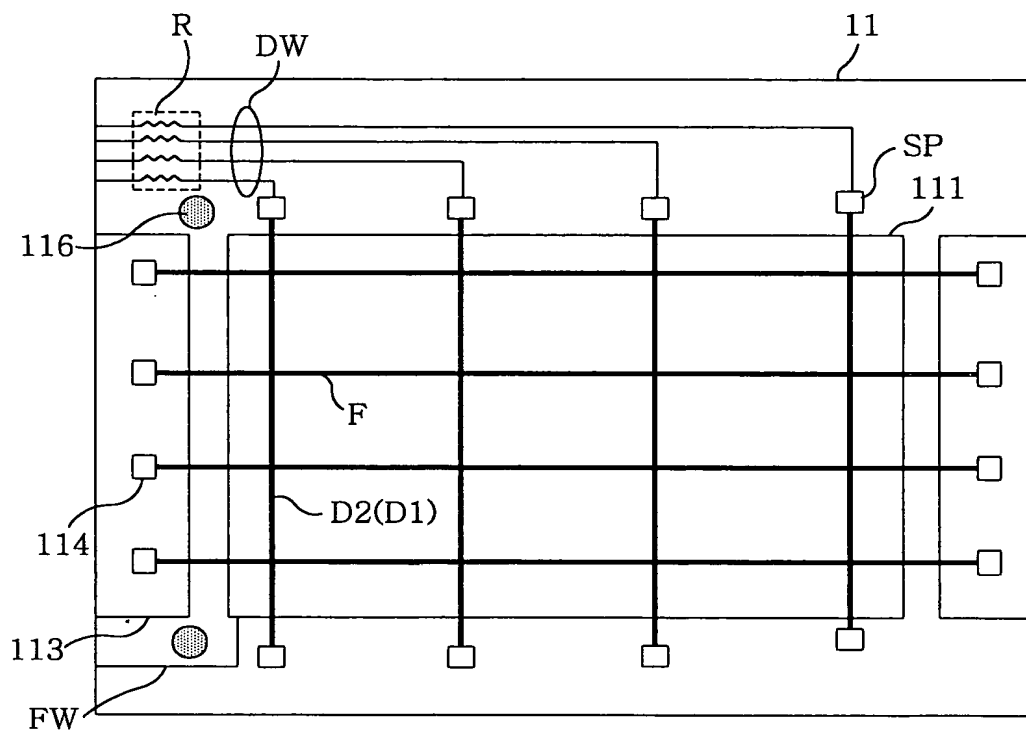


FIG. 11A
(PRIOR ART)

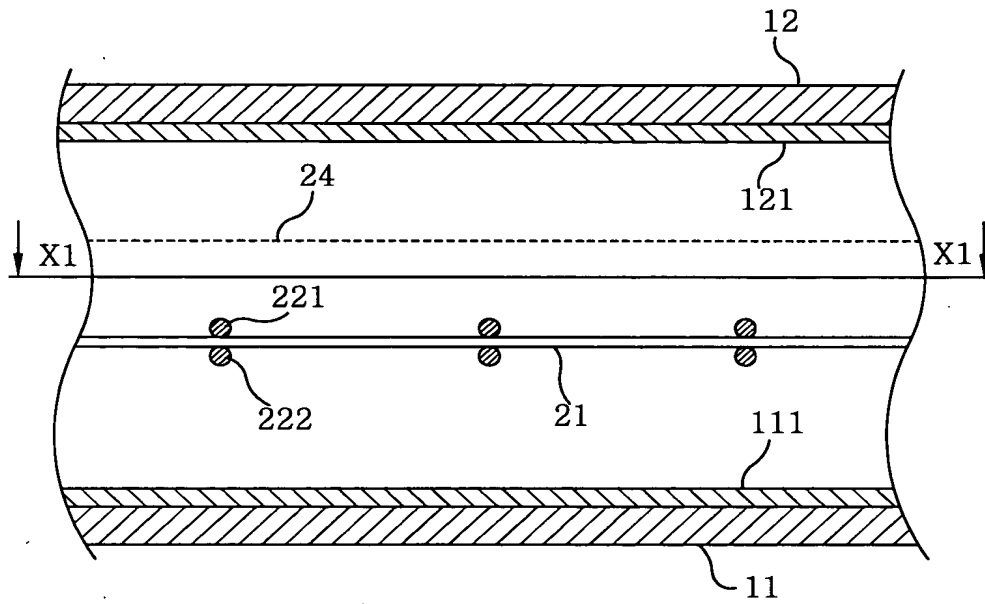


FIG. 11B
(PRIOR ART)

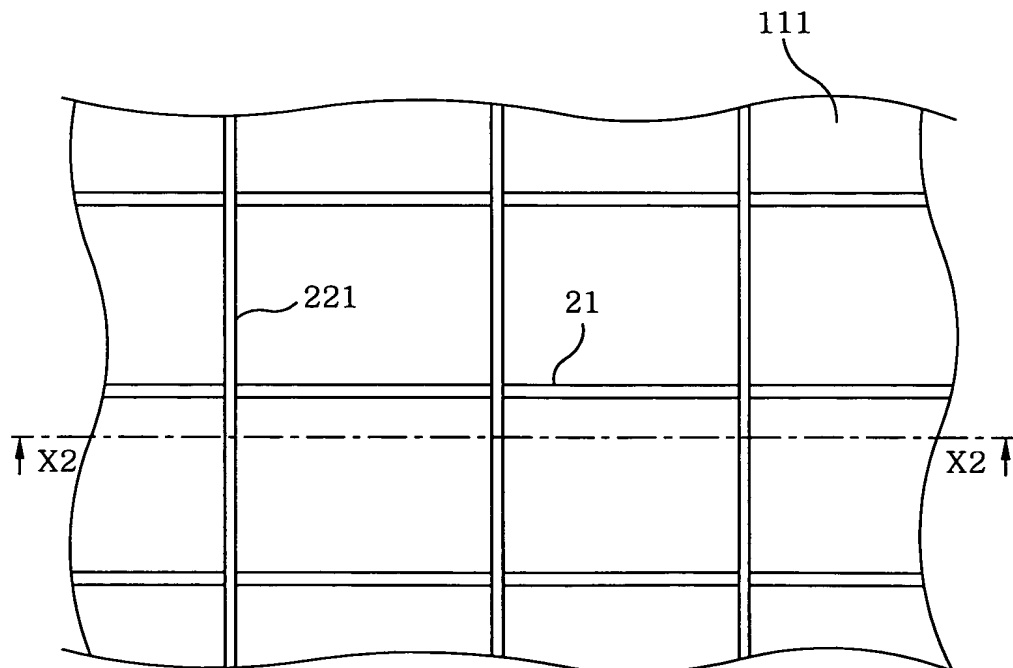


FIG. 12A
(PRIOR ART)

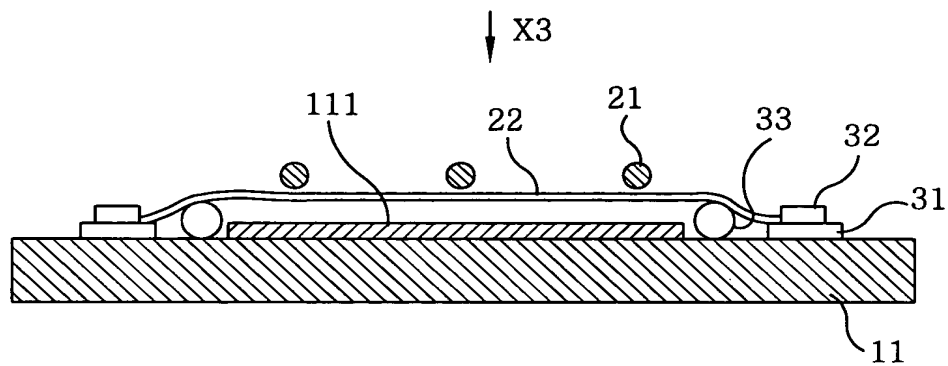


FIG. 12B
(PRIOR ART)

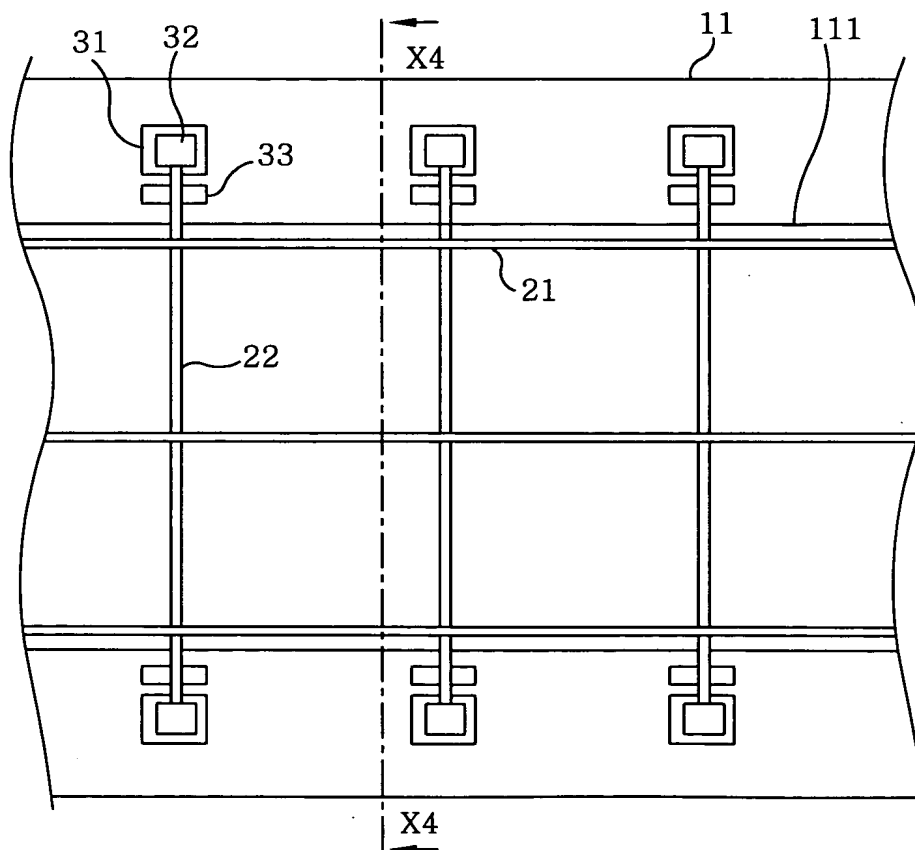


FIG. 13

